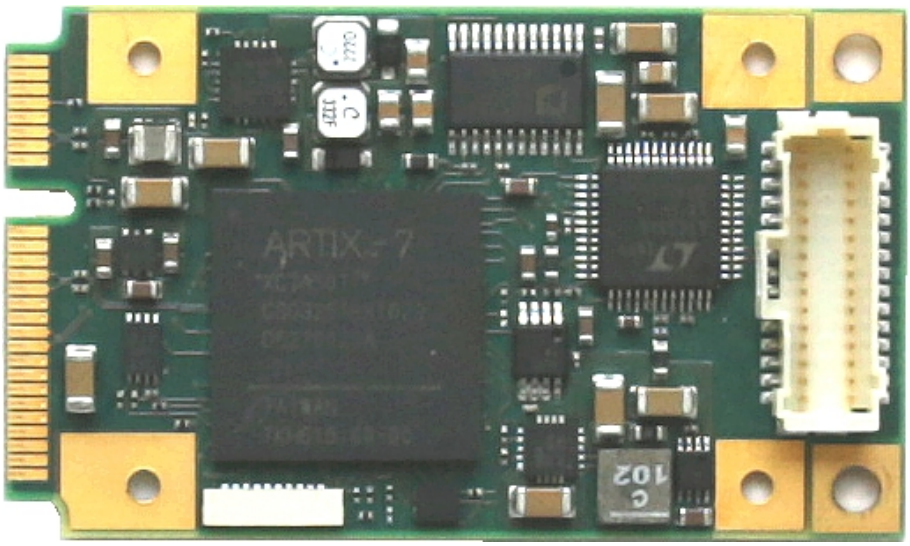
The Embedded I/O Company

TMPE627 Reconfigurable FPGA with AD/DA & Digital I/O PCIe Mini Card



TMPE627-10R

Application Information

The TMPE627 is a standard full PCI Express Mini Card, providing a user programmable Xilinx Artix-7 7A50T FPGA.

The TMPE627 provides 14 ESD-protected 5 V-tolerant TTL lines. All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate. Each TTL I/O line has a pull-resistor to a common programmable pull-up voltage that can be set so +3.3 V, +5 V and GND.

The 16 bit ADC offers 4 input channels that can be software configured to operate in single-ended or differential mode. It offers software selectable input voltage ranges of 0-5.12 V, 0-10 V, 0-10.24 V, ±5 V, ±5.12 V, ±10 V and ±10.24 V with a sampling rate of up to 200 ksps.

The DAC offers 4 channels of 16 bit analog outputs with software selectable output voltage ranges of 0-5 V, 0-10 V, 0-10.8 V, ±5 V, ±10 V or ±10.8 V. The output voltage range can be individually set per channel. The conversion time is typ. 10 µs and the DAC outputs are capable to drive a load of 2 kΩ, with a capacitance up to 4000 pF.

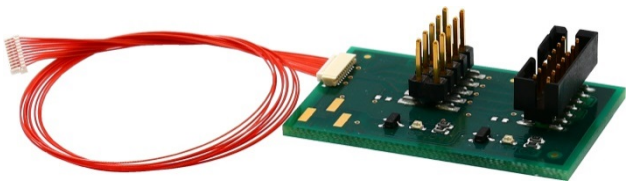
Each TMPE627 is factory calibrated. The calibration information is stored in an on-board serial EEPROM unique to each TMPE627 module.

The I/O signals are accessible through a 30 pin Pico-Clasp latching connector.

The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using the Vivado ILA). With the TA308 Programming Kit direct JTAG access to the FPGA is possible, using the Xilinx Platform Cable USB.

User applications for the TMPE627 with 7A50T FPGA can be developed using the design software Vivado Design Suite HL WebPACK Edition, which can be downloaded free of charge from www.xilinx.com.

TEWS offers a well-documented basic FPGA Example Application design. It includes a constraints file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE627. It implements PCIe to register mapping and basic I/O. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream.



TA308

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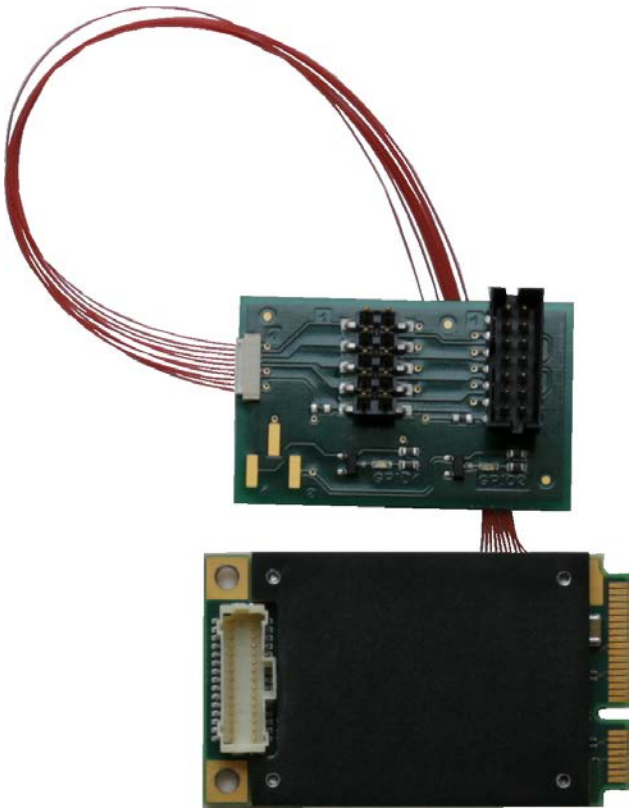
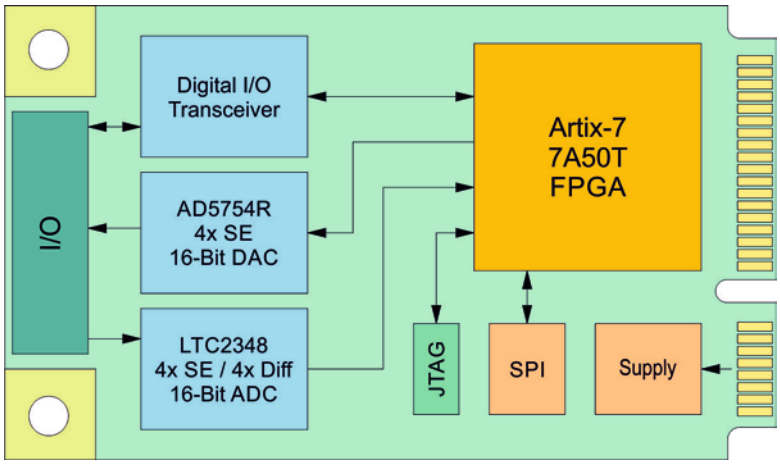


TA308 with TMPE627

Technical Information

- Form Factor: Full-Mini Card
  - Board size: 50.95 mm x 30 mm
  - PCI Express 1.1 compliant interface
- Artix-7 User programmable FPGA
  - TMPE627-10R: Xilinx XC7A50T-2
  - PCIe endpoint in FPGA
- 128 Mbit SPI-EEPROM for FPGA configuration and User Data
- Digital I/O
  - 14 ESD-protected 5 V-tolerant TTL lines with programmable pull- resistor
  - Direction individually programmable
- 4 channels 16 bit analog input
  - Simultaneous sampling
  - True differential inputs
  - Programmable input voltage (one setting for all channels):
    0-5.12 V, 0-10 V, 0-10.24 V,
    ±5 V, ±5.12 V, ±10 V, ±10.24 V
  - Sampling rate: 200 kSPS
  - Overvoltage protection
  - Factory calibration
- 4 channels single-ended 16 bit isolated analog output
  - Simultaneous update
  - Programmable output voltage:
    0-5 V, 0-10 V, 0-10.8 V,
    ±5 V, ±10 V, ±10.8 V
  - Conversion time: typ.10 µs
  - Up to 2 kΩ resistive, 4000 pF capacitive load
  - Overcurrent protection
  - Factory calibration
- I/O access
  - 30 pin Pico-Clasp latching connector
- MTBF (MIL-HDBK217F/FN2 GB 20°C)
  TMPE627: 987.000 h



TMPE627 Block Diagram

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Order Information

RoHS Compliant

TMPE627-10R 14 TTL I/O, 4 AD, 4 DA, Artix-7 7A50T FPGA

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TMPE627-DOC User Manual

Software

For Software Support please contact TEWS.

Related Products

TA308 Cable Kit for Modules with XRS JTAG Connector

TA309 Cable Kit for Modules with Pico-Clasp Connector

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